

Figure 1

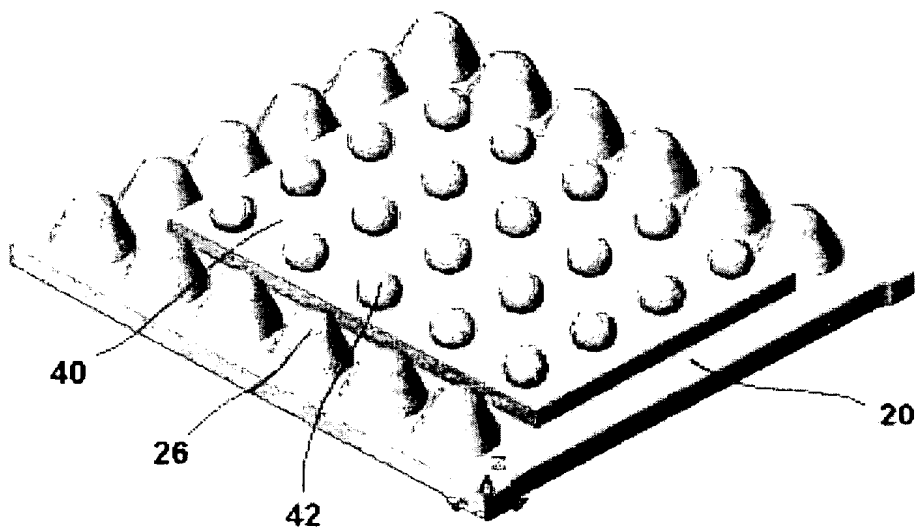


Figure 2.

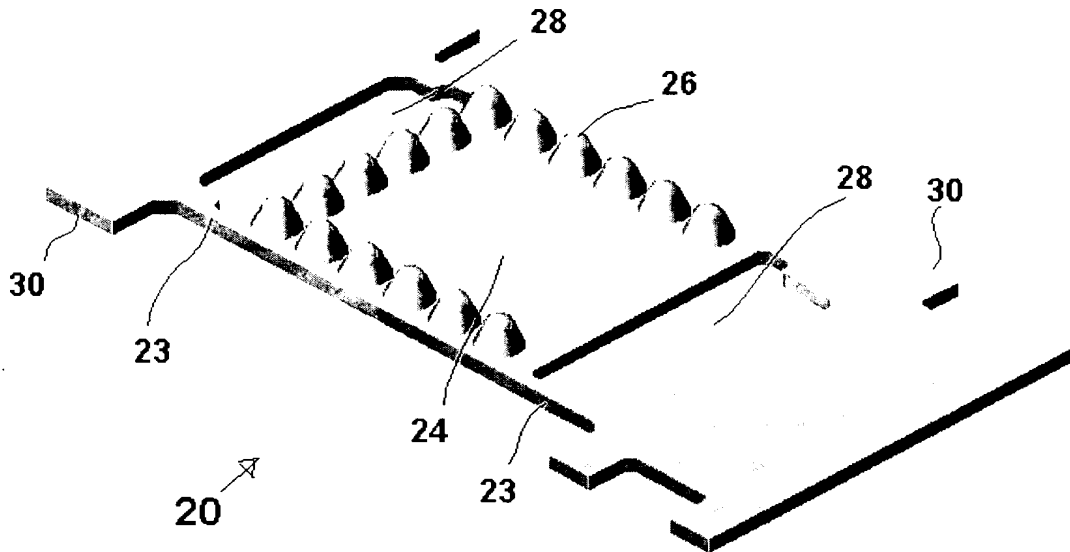


Figure 3.

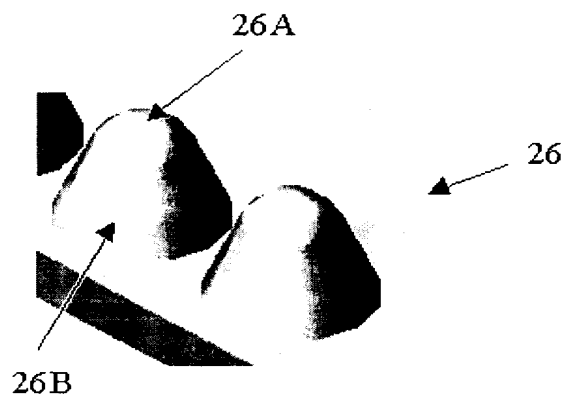


Figure 4

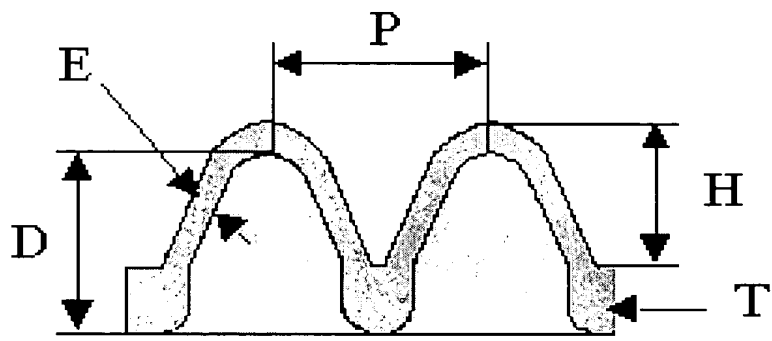


Figure 5

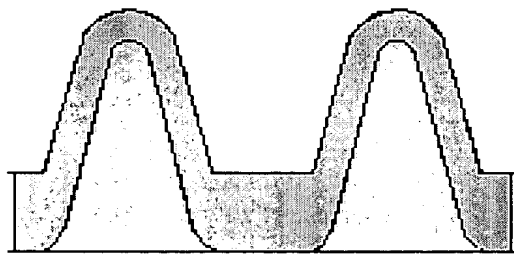


Figure 6

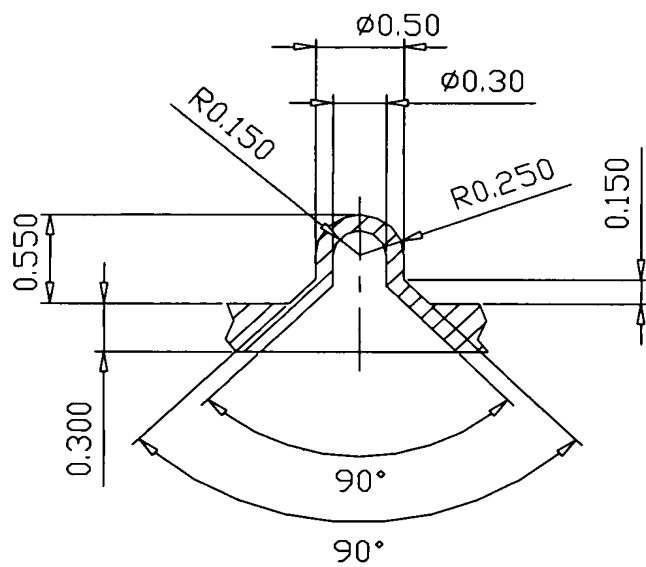


Figure 7

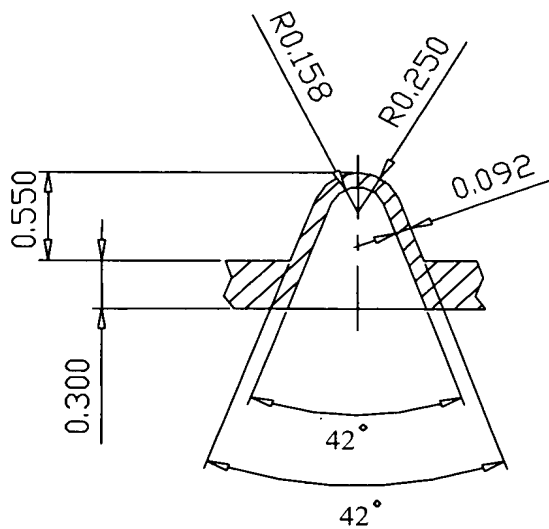


Figure 8

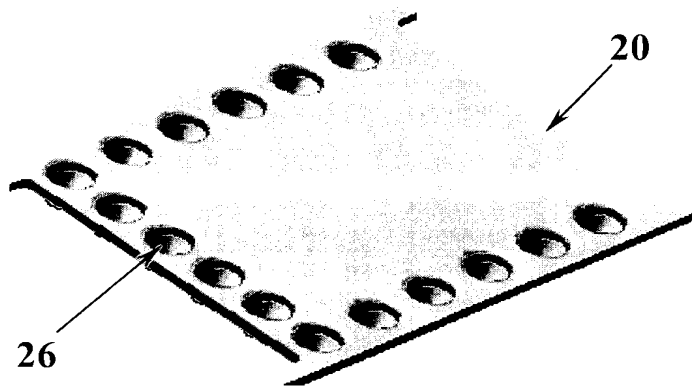


Figure 9

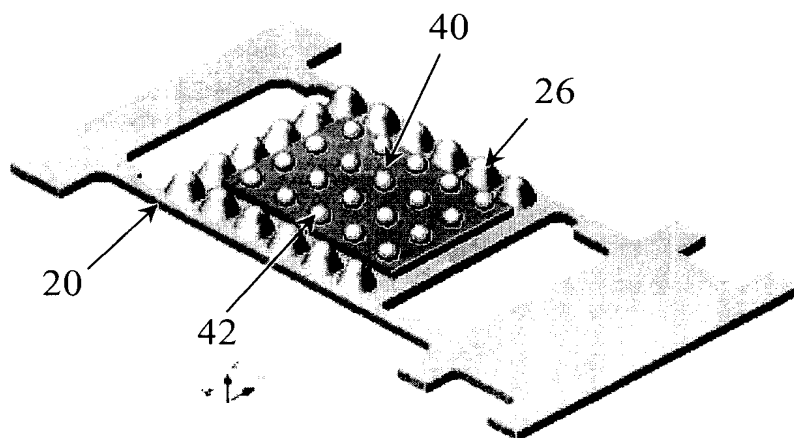


Figure 10

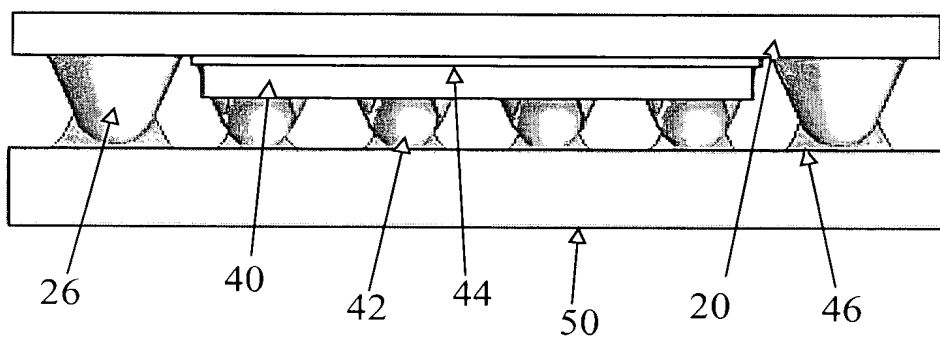


Figure 11

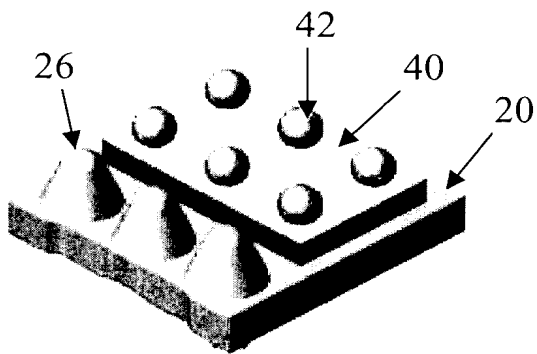


Figure 12a

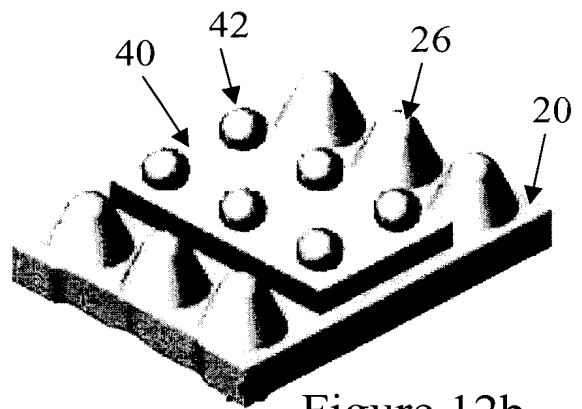


Figure 12b

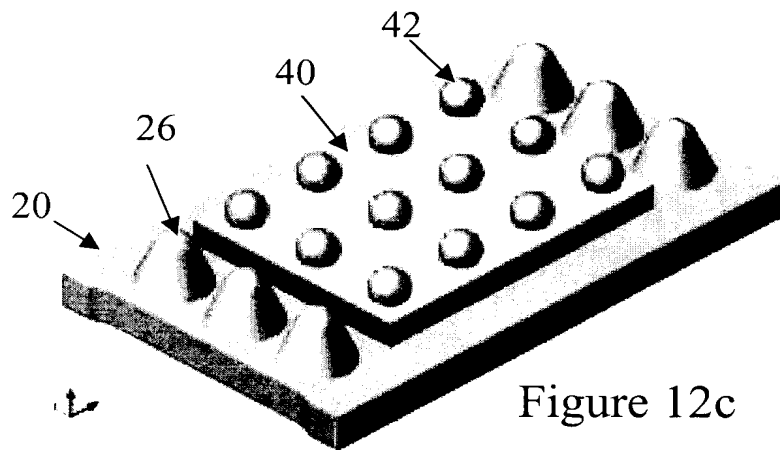


Figure 12c

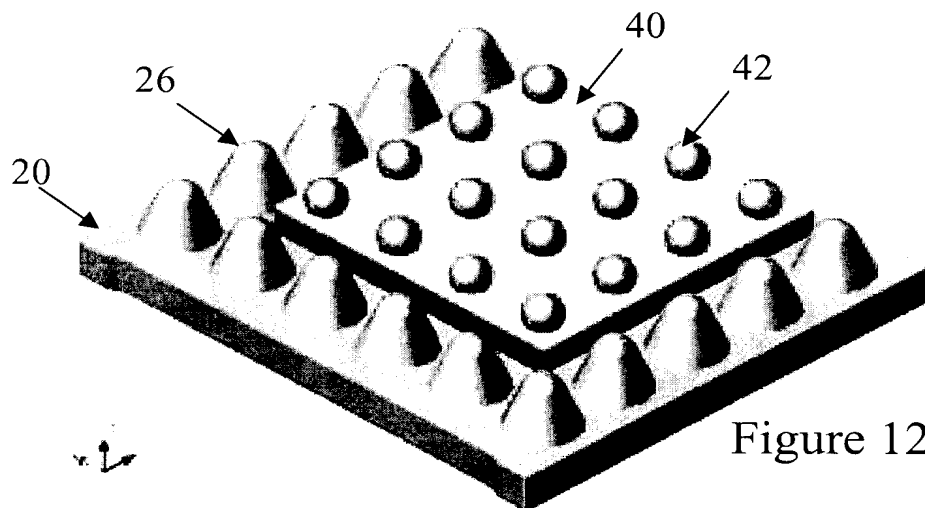


Figure 12d

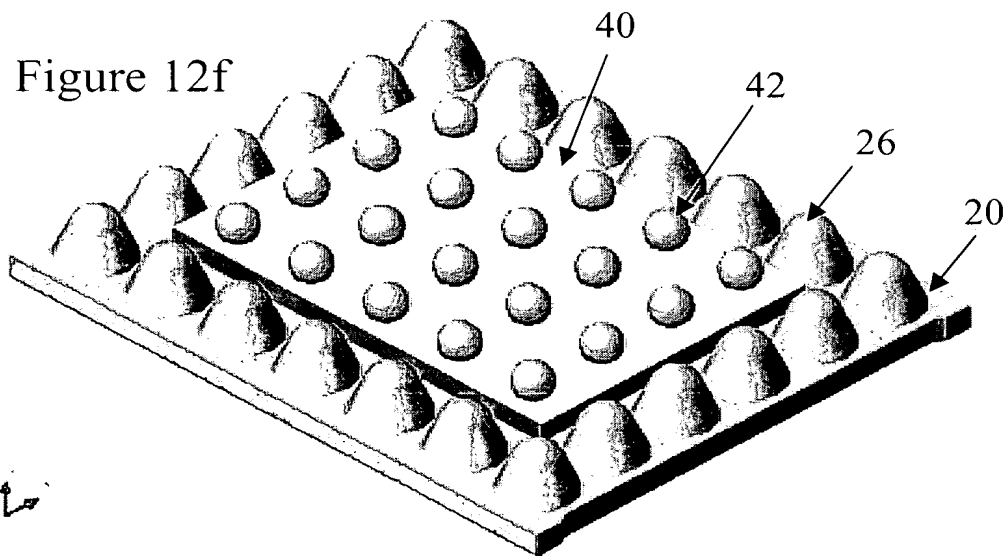
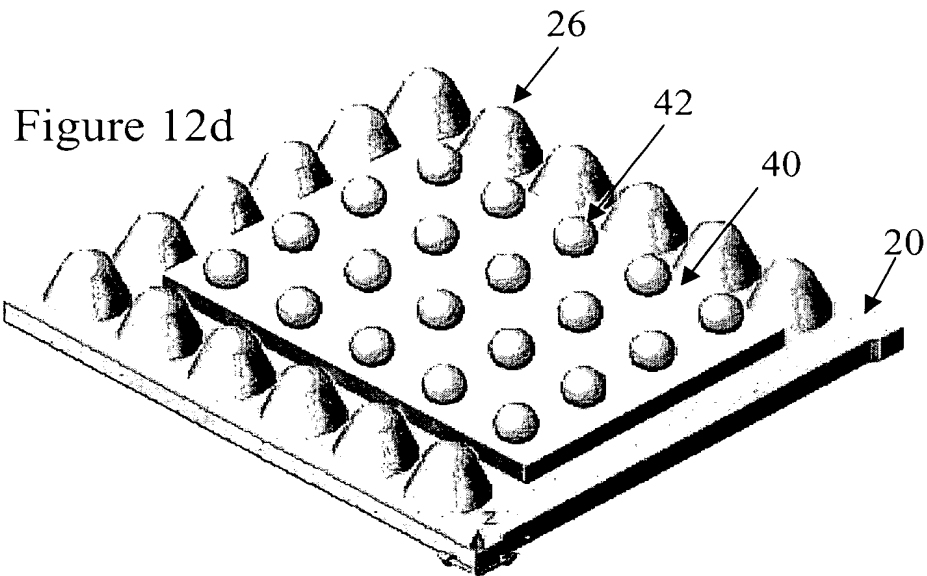


FIG. 13 is a perspective view of a semiconductor device 10 in accordance with the present invention. The device 10 includes a substrate 15, a gate 20, a gate 20-1, a gate 20-2, a gate 26, a gate 26-G, a gate 40, a gate 42, a gate 42-G, and a gate 42-G.

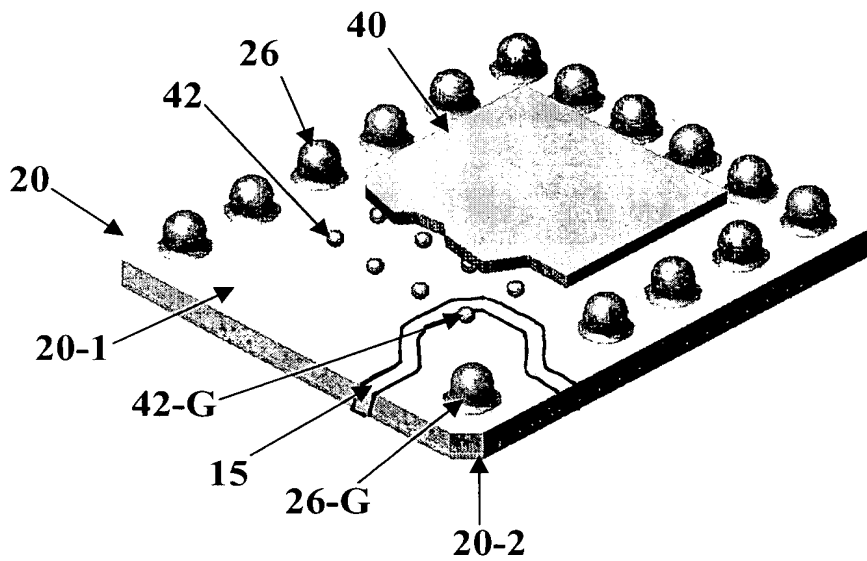


Figure 13

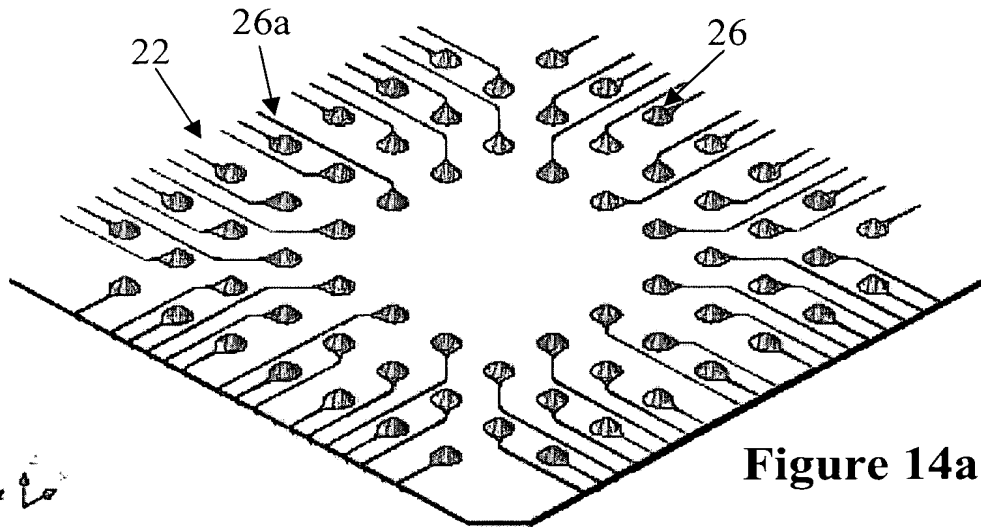


Figure 14a

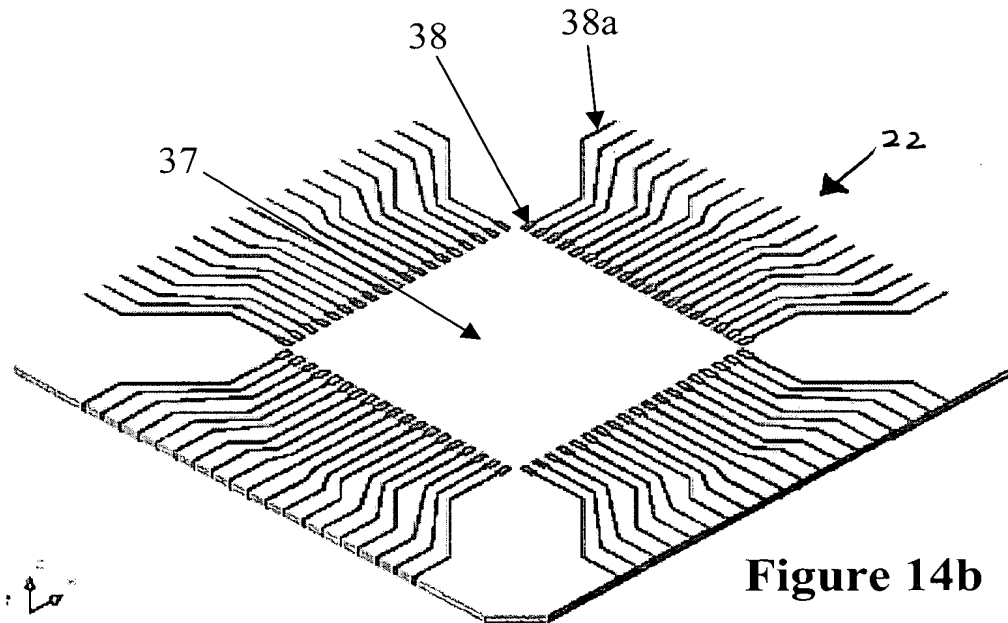


Figure 14b

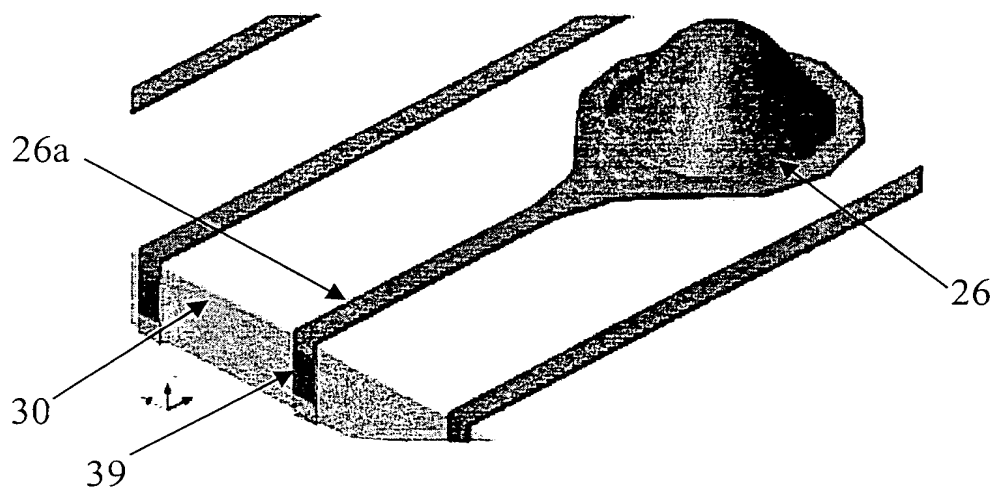


Figure 14c

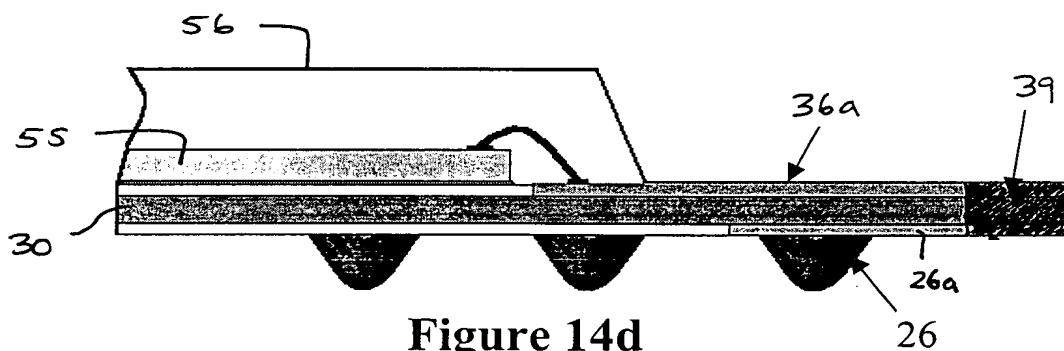


Figure 14d

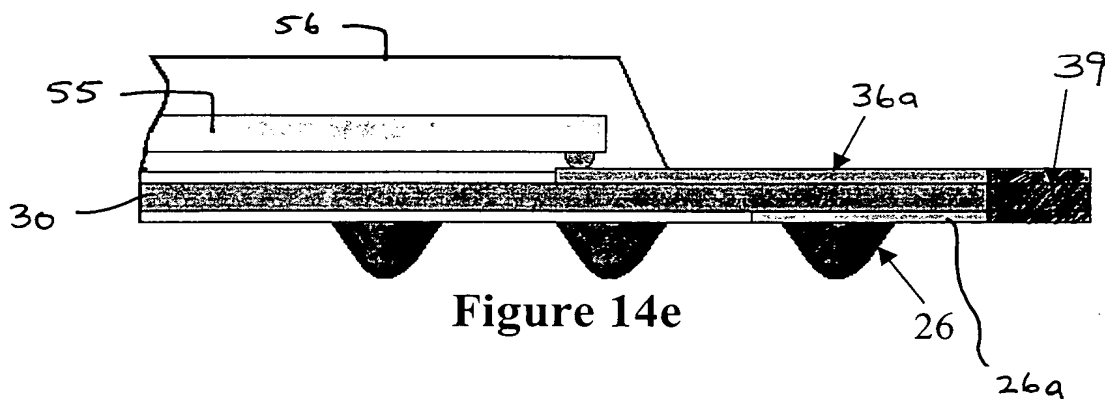


Figure 14e

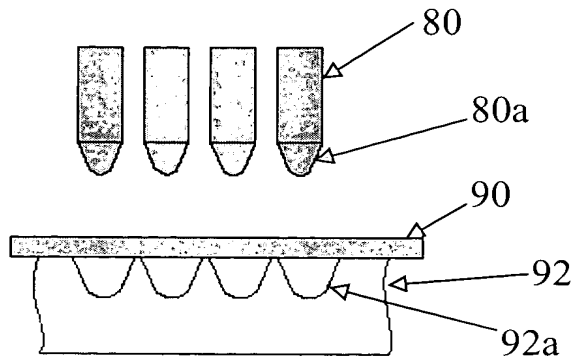


Figure 15a

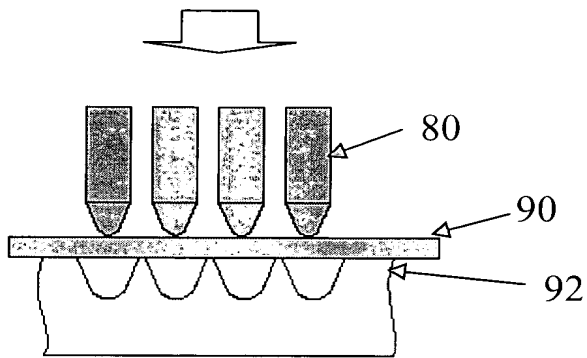


Figure 15b

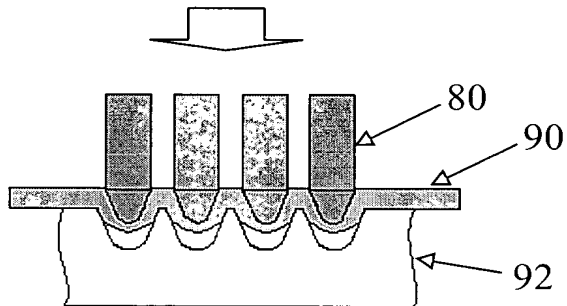


Figure 15c

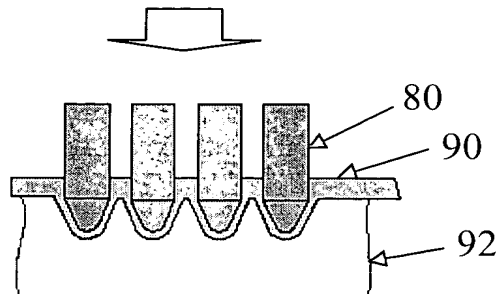


Figure 15d

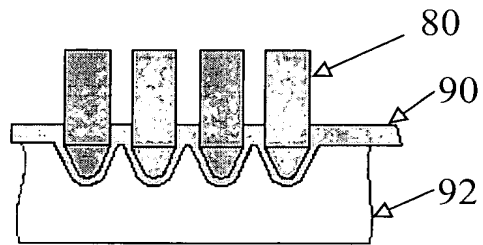


Figure 15e

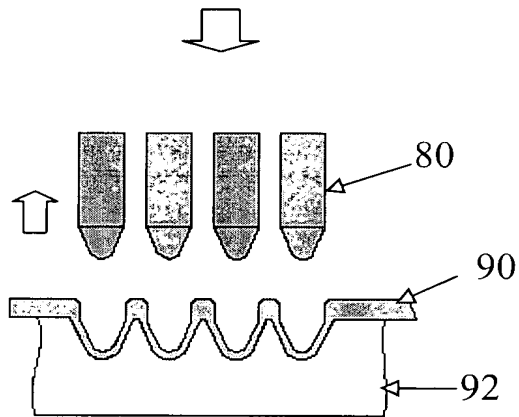


Figure 15f

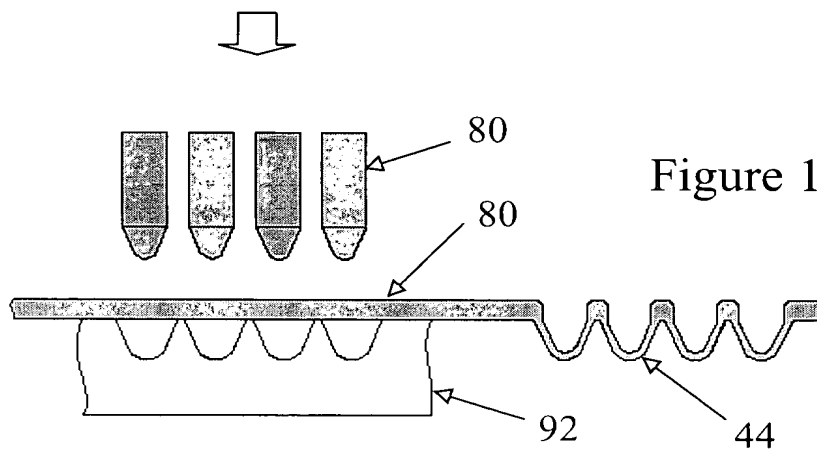


Figure 15g

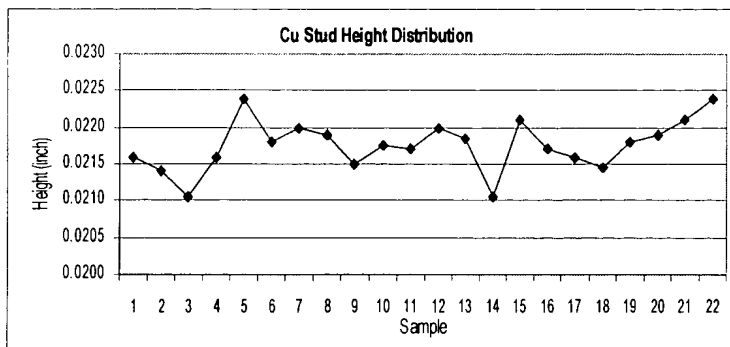


Figure 16

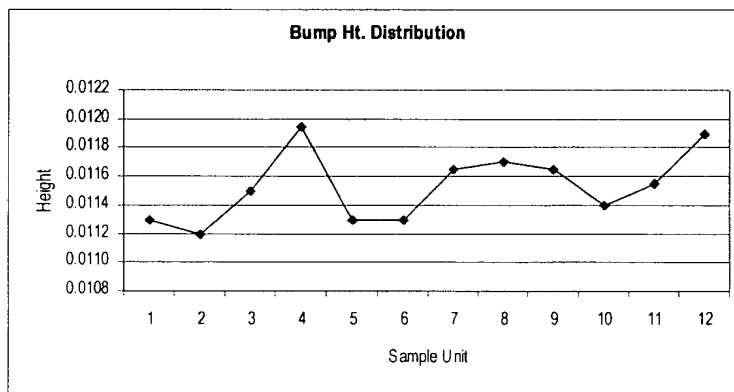


Figure 17

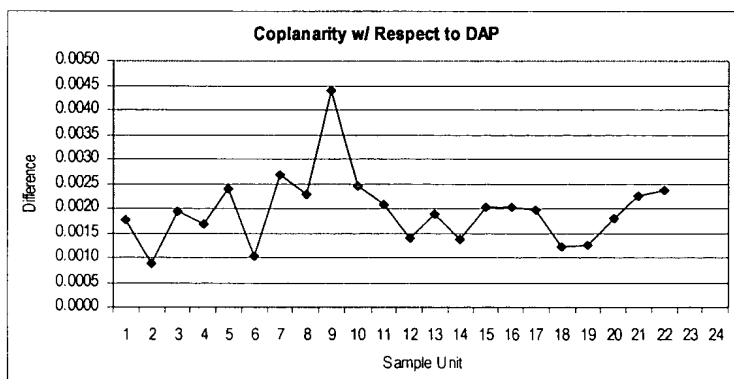


Figure 18

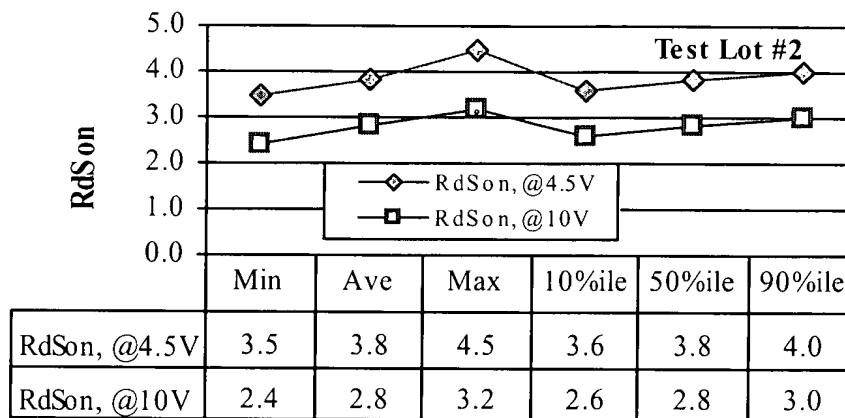


Figure 19

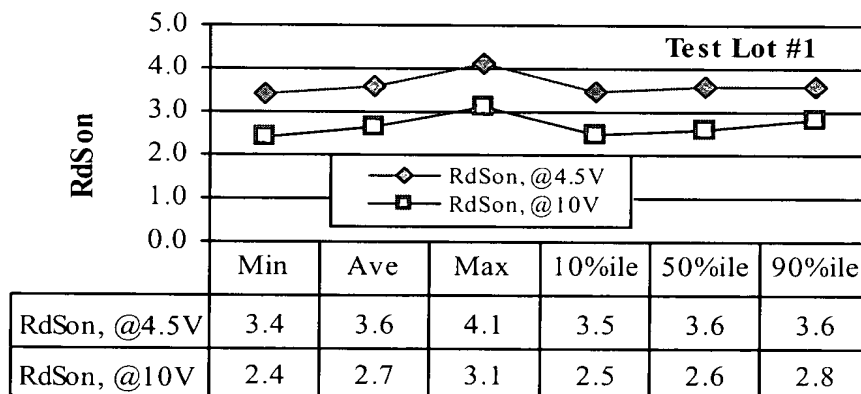


Figure 20